REMARKS

Claims 1-27 are all of the claims pending in the present Application. Applicant gratefully acknowledges the Examiner's indication that claims 3, 13, 15, and 18 would be allowable, if rewritten in independent format and has accordingly rewritten claims 3 and 13 in independent format. However, Applicant believes the independent claims are fully allowable when properly understood and, therefore, declines to rewrite these claims in independent format at this time.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1 and 21 stand rejected under 35 USC §112, second paragraph, as being indefinite. Applicant believes the above claim amendments address the Examiner's concern and requests that the Examiner reconsider and remove this rejection.

Claim 1 stands rejected under 35 USC §102(e) as anticipated by US Patent 6,320,229 to Uchikoba et al. Claim 2 stands rejected under 35 USC §103 (a) as being unpatentable over Uchikoba, further in view of US Patent 5,324,982 to Nakazato et al. Claims 2, 4-12, 14, 16, 17, and 29-27 stand rejected under 35 USC §103 (a) as being unpatentable over Uchikoba, further in view of Applicant's Admitted Prior Art.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, for example by claim 1, the present invention is directed to an input/output protection device for a semiconductor integrated circuit having a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring. A first region of a first diffusion layer is fabricated in a region of the first conduction type of the semiconductor substrate. The first diffusion layer has a second conduction type opposite the first conduction type. The first region is connected to the input/output terminal;

A second region of the first diffusion layer of the second conduction type is held at a predetermined potential. A third region having a diffusion layer of the second conduction type is fabricated at a bottom of the second region. The third region is connected to the second region of the first diffusion layer. The third region is fabricated at a location other than at a bottom of the first diffusion layer of the first region.

The first region is circularly enclosed by the second and third regions, and the first,

second, and third regions form a parasitic transistor in which the first region serves as a collector and the second and third region serve as an emitter.

Advantages of the present invention include that an overvoltage at the input terminal causes a rapid turn-on of the lateral NPN transistor comprising the first, second, third, and fourth regions, in conjunction with the substrate. The rapid speed is caused by the blocking action of the third region of carriers, which blocking action allows voltage to quickly build up in the base of the lateral transistor.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Uchikoba anticipates claim 1 and, when combined with Nakazato, renders claim 2 obvious. The Examiner further alleges that Uchikoba, when combined with Applicant's Admitted Prior Art renders obvious claims 2, 4-12, 14, 16, 17, and 19-27. Applicant disagrees.

First, relative to the rejection for claim 1, Uchikoba Figure 5 shows a ringed-shaped n-well structure 24 connected to a high potential pad VDP. This n-well structure 24 does not serve as an emitter on a parasitic bipolar transistor.

In contrast, the present invention provides a first region corresponding to a collector of a parasitic bipolar transistor. A second region and a third region circularly encloses the first region and serve as the emitter for the parasitic bipolar transistor.

The present invention provides a lateral NPN parasitic bipolar transistor so that an overvoltage at the input terminal causes a rapid turn-on of the lateral NPN transistor. The rapid speed is caused by the blocking action of the third region of carriers, which blocking action allows voltage to quickly build up in the base of the lateral transistor.

The prior art fails to teach this rapid turn-on technique for input terminal protection.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of: "... said first region, said second region, and said third region thereby forming a parasitic bipolar transistor in which said first region serves as a collector thereof and said second region and said third region serve as an emitter thereof", as required by claim 1.

Relative to the rejection for claim 2, the Examiner concedes that Uchikoba fails to teach or suggest a fourth region, having the same conductivity type as the substrate, below the first region. To overcome this deficiency, the Examiner introduces Nakazato and alleges that one of ordinary skill in the art would have been motivated to modify Uchikoba to incorporate a fourth diffusion layer corresponding to region 102 of Figure 16 of Nakazato "to prevent minority carriers from entering the memory cell or from entering the semiconductor region electrically connected to the bit line."

There are several problems with the Examiner's reasoning. First, as pointed out above, Uchikoba fails to have the parasitic transistor structure described by claim 1.

Second, Nakazato relates to a DRAM memory unit, which is a totally different circuit from the surge protection circuit shown in Uchikoba. Therefore, there is no reason to modify Uchikoba to "prevent minority carriers from entering the memory cell" when Uchikoba has no such memory cells nor suggests to interconnect to such memory cells as the Examiner seems to presume. Nor does Nakazato suggest interconnecting region 102 to a voltage surge protection circuit.

Without some suggestion in the prior art itself, the combination urged in the rejection of record is improper under MPEP §2143.01: "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination." (Emphasis in MPEP itself)

Third, the DRAM circuit of Nakazato is clearly incompatible with the surge circuit shown in Uchikoba. Nakazato contains diffusion layers and wells and transistor structures that are not present in Uchikoba. It is an entirely different circuit. Merely selecting the diffusion region 102 from Nakazato, totally out of context from the prior art circuit, does not meet the burden of a *prima facie* rejection and is clear evidence of impermissible hindsight.

In order to meet such burden, the rejection would have to start with the structure of the primary reference Uchikoba and provide a rationale to convert the n-well structure into a parasitic transistor. No such rationale reasonably exists in the rejection of record, let alone the references themselves.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of: "... said first region, said second region, and said third region thereby forming a parasitic bipolar transistor in which said first region serves as a collector thereof and said second region and said third region serve as an emitter thereof", as required by claim 1.

Furthermore, there is no teaching or suggestion of: "... wherein the region of the first conduction type of the semiconductor substrate includes a fourth diffusion layer having an impurity concentration higher than that of the semiconductor substrate", as required by claim 2.

Moreover, the rejection based on Uchikoba, further in view of the Applicant's Admitted Prior Art, fails to meet the initial burden of a *prima facie* rejection, for the same reasons discussed above for the rejection based on Uchikoba/Nakazato.

That is, as pointed out above, the circuit of Uchikoba does not have a parasitic transistor structure, but, instead, uses a concept in which an n-well guard ring 24,34 is connected to high potential VDP. Therefore, relative to claims 1-20 and 27, Uchikoba cannot be used as the primary reference in combination with Applicant's Admitted Prior Art, since

such combination would change the principle of operation of the primary reference.

Relative to the rejection for claims 21-26 based on this combination of Uchikoba/Applicant's Admitted Prior Art, the combination urged by the Examiner cannot be considered by one of ordinary skill in the art as being reasonable, since the insertion of a p-well structure into Uchikoba Figure 5 would destroy the operation of that circuit.

Further, the other prior art of record has been reviewed, but it too, even in combination with Uchikoba, Nakazato, or Applicant's Admitted Prior Art, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-27, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 8/12/03

Frederick E. Cooperrider
Reg. No. 36,769

McGinn & Gibb, P.C.
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254